Xilinx® ISE Simulator (ISim) with Verilog Test Fixture Tutorial

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Overview

This tutorial provides instruction for using the basic features of the Xilinx ISE simulator with the WebPACK environment. This tutorial uses Verilog test fixture to simulate an example logic circuit.

More detailed tutorials for the Xilinx ISE tools can be found at http://www.xilinx.com/support/techsup/tutorials/

Getting Started

You first need to install Xilinx ISE WebPACK on your PC or laptop. The latest version of the software is currently 11.1, which is what we use in this tutorial. It is available as a free download from www.xilinx.com.

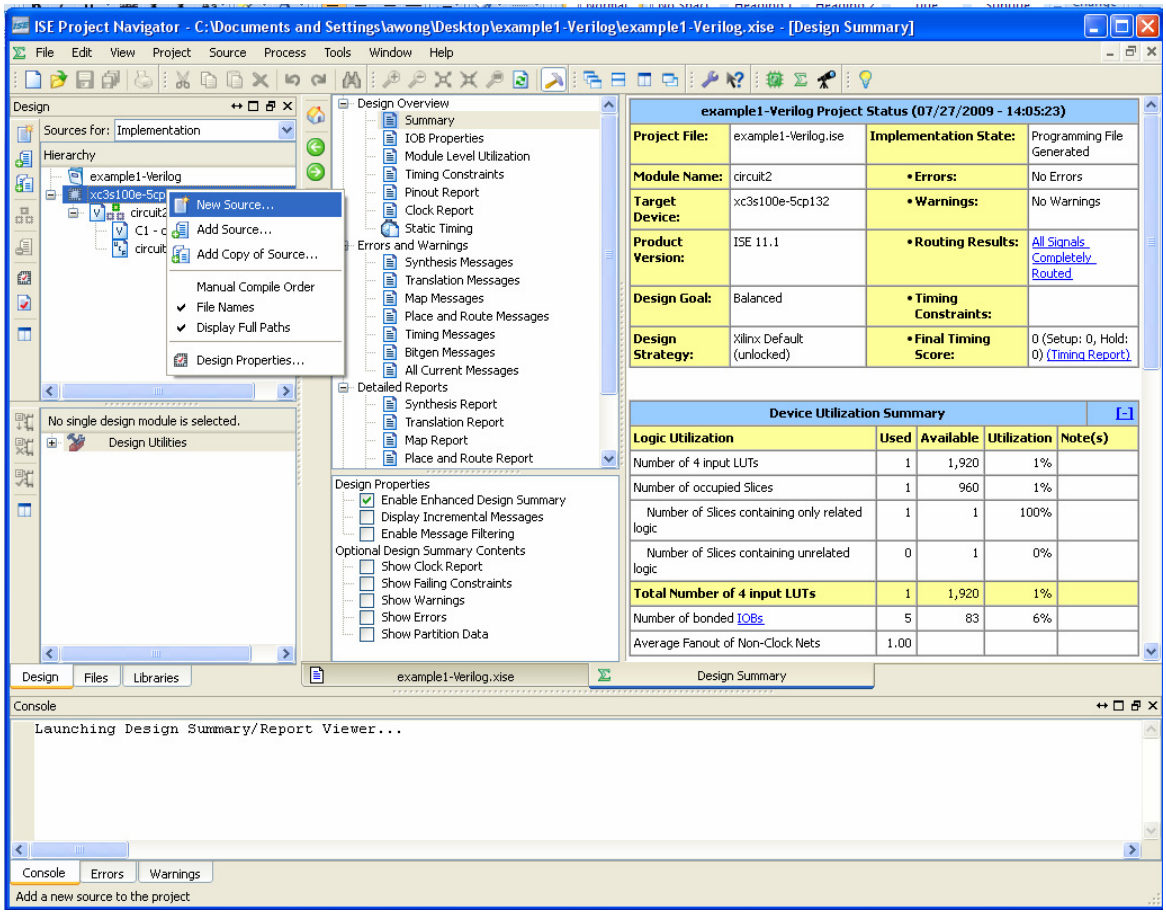
This tutorial uses the project example1-Verilog, from another Digilent tutorial on the Xilinx ISE WebPACK tools. This project is available as a free download from www.digilentinc.com.

Starting Sample Project

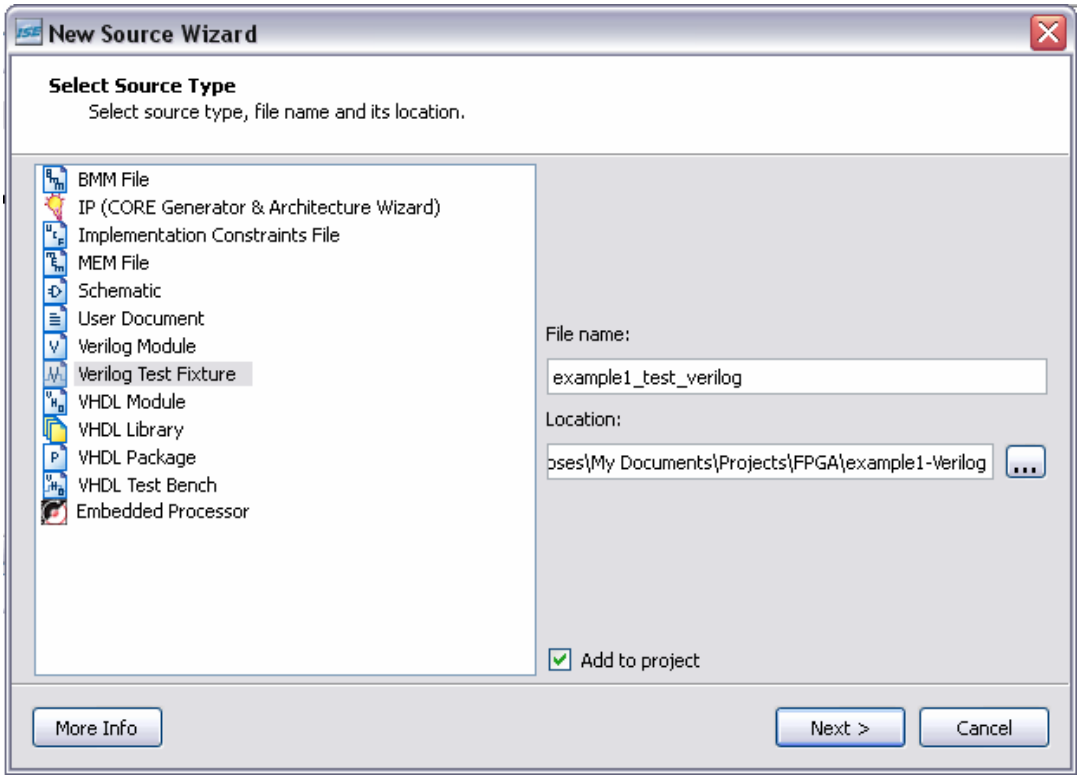
First, open Project Navigator by selecting Start > Programs > Xilinx ISE Design Suite 11 > ISE > Project Navigator. Once the application opens, specify an ISE project file by selecting File > Open Project and navigate to the appropriate directory to choose your project. In this tutorial, we use example1-Verilog.xise

Once the project is open, add a Verilog Test Fixture source file to your project. In this source file, you are able to define circuit inputs over time so the simulator knows how to drive the outputs.

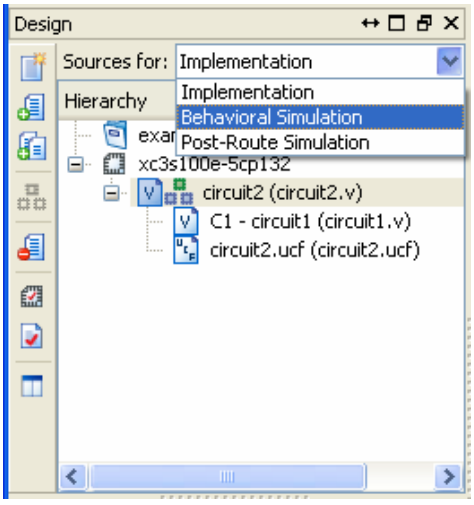
To add the source file, right-click on the device in the Sources window and choose the New Source option. In the New Source wizard, choose VHDL test fixture for the source type and enter a meaningful name for the file. We call ours “example1_test_verilog”.



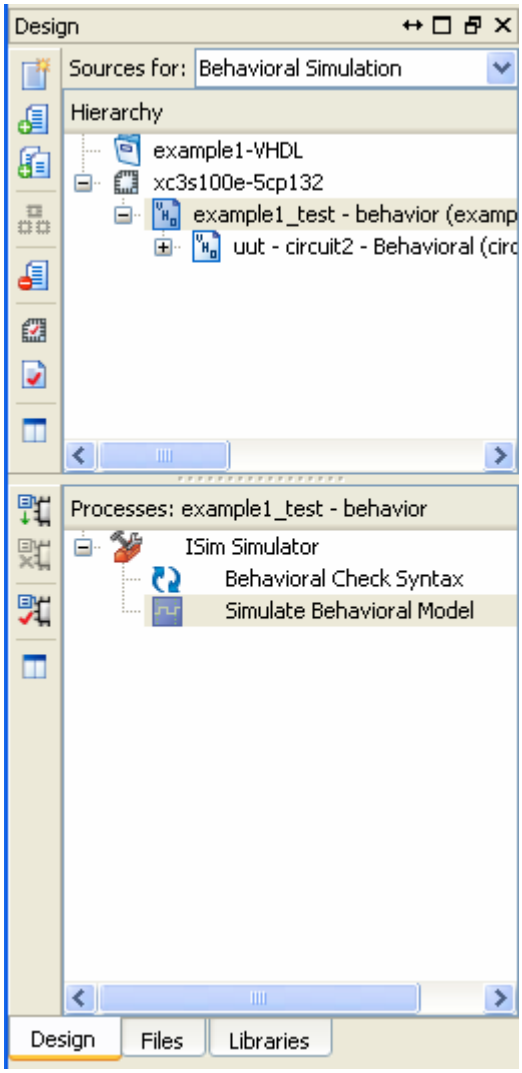
After clicking Next, the following dialog box asks you to select the source file you want to associate with the given test fixture file. This dictates which source file you actually run the simulation on. In this tutorial, we run the simulation on the top-level module of the example1-VHDL design (circuit2.v).



Complete the new source file creation by clicking Next and Finish. To view and edit the Verilog test fixture, you first need to change the selected option in the sources drop-down menu from Implementation to Behavioral Simulation as follows:



Once this option is selected, the sources panel changes slightly so that example1_test_verilog.v is the first source file under the device. The options under the processes panel change so that the only option is the ISim Simulator (sic).



Verilog Test Fixture

Open the Verilog test fixture in the HDL editor by double-clicking it in the Sources window. If you examine the contents of the new source file you will see that, like a standard VHDL source file, the Xilinx tools automatically generate lines of code in the file to get you started with circuit input definition. This generated code includes:

- a Comment block template for documentation
- a Module statement
- a UUT instantiation
- input initialization

Scroll down to the end of the test fixture file to see the "initial begin" and "end" statements of the module.

```
24
25  module example1_test_verilog;
26
27     // Inputs
28     reg AT;
29     reg BT;
30     reg CT;
31     reg DT;
32
33     // Outputs
34     wire YT;
35
36     // Instantiate the Unit Under Test (UUT)
37     circuit2 uut (
38        .AT(AT),
39        .BT(BT),
40        .CT(CT),
41        .DT(DT),
42        .YT(YT)
43     );
44
45     initial begin
46        // Initialize Inputs
47        AT = 0;
48        BT = 0;
49        CT = 0;
50        DT = 0;
51
52        // Wait 100 ns for global reset to finish
53        #100;
54
55        // Add stimulus here
56
57     end
58
59  endmodule
```

The simplest way of defining input stimulus in a Verilog test fixture is to use timing controls and delay, denoted by the pound symbol (#). For example, the statement #100 present in example1_test_verilog.v tells the simulator to delay for 100 ns. Therefore, any statement made after this timescale statement will occur after the 100 ns delay time.

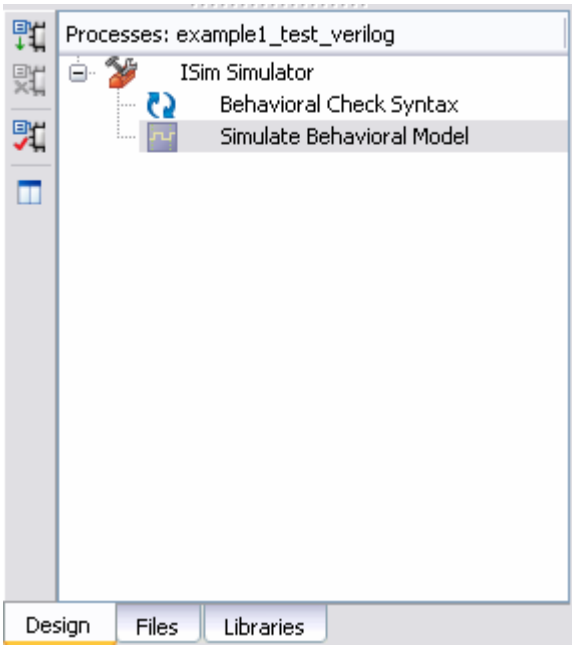
It's important to note that the timescale for the delay is defined by the `timescale statement at the beginning of the file. By default, the Xilinx tools define the timescale as 1ns/1ps, which indicates that the units are in nanoseconds while calculated time precision is 1 picoseconds.

To add further input stimulus, we will add the several more statements until the completed verilog test fixture looks like this:

```
32
33      // Outputs
34      wire YT;
35
36      // Instantiate the Unit Under Test (UUT)
37      circuit2 uut (
38          .AT(AT),
39          .BT(BT),
40          .CT(CT),
41          .DT(DT),
42          .YT(YT)
43      );
44
45      initial begin
46          // Initialize Inputs
47          AT = 0;
48          BT = 0;
49          CT = 0;
50          DT = 0;
51
52          // Wait 100 ns for global reset to finish
53          #100;
54
55          #10 AT = 1;
56
57          #10 BT = 1;
58
59          #10 AT = 0;
60              CT = 1;
61
62          #10 DT = 1;
63
64
65
66          // Add stimulus here
67
68      end
69
70  endmodule
```

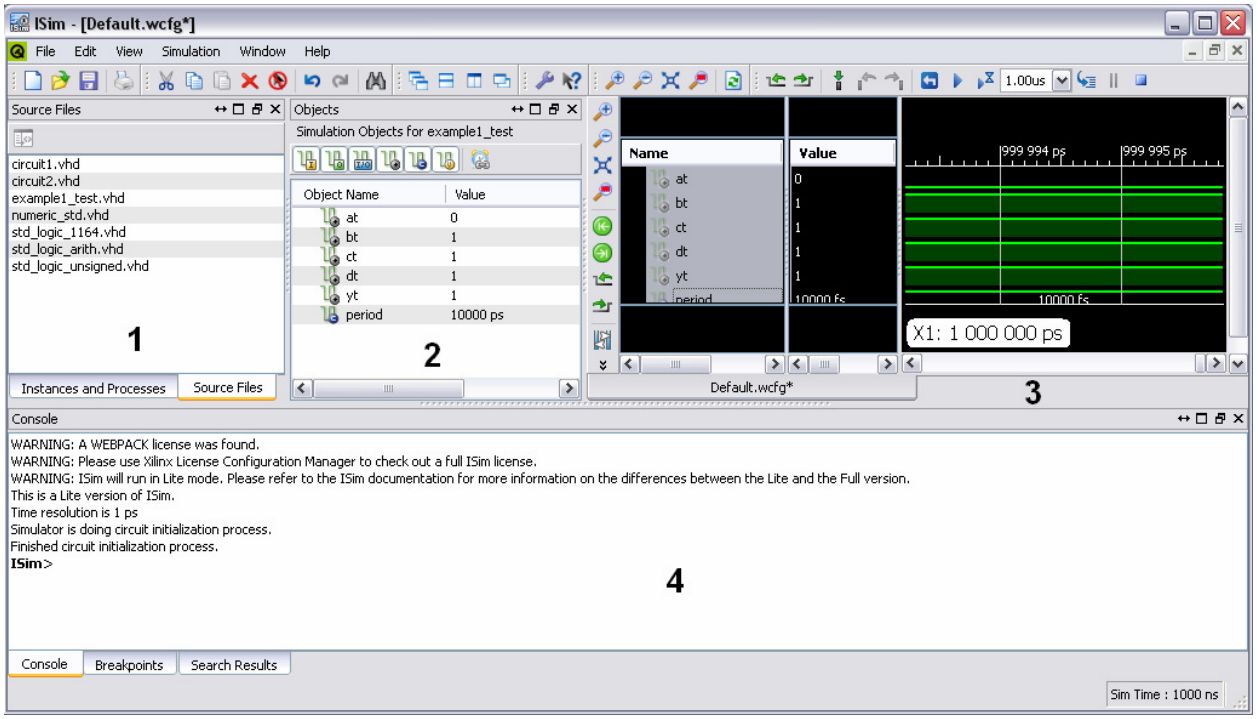
Note that the assignment statements take place in the simulation after each delay. The inputs then stay at their respective states until assigned otherwise.

Now, save the test fixture and select it in the sources window. Go to the processes window, expand the ISim Simulator (sic), and double-click Simulate Behavioral Model.



ISE Simulator

Running the Simulate Behavioral Model process causes the ISim window to appear.

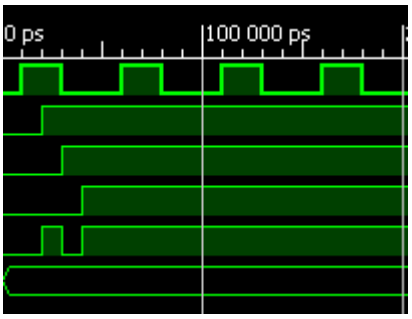


Some features of this window include:

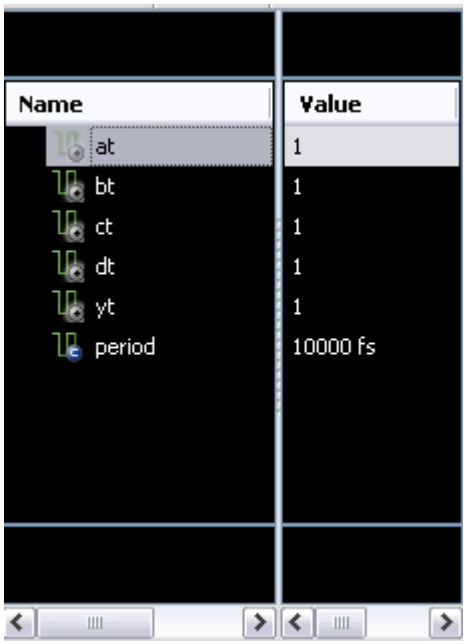
1. a Source Files panel where source files to be viewed can be selected
2. an Objects panel where different signals can be added to the simulation
3. a simulation panel where the state of signals can be observed
4. a Console panel

We first use the Zoom to Full View tool to see the full view of the simulation, which is located to the right of the magnifying glasses on the simulation panel toolbar.

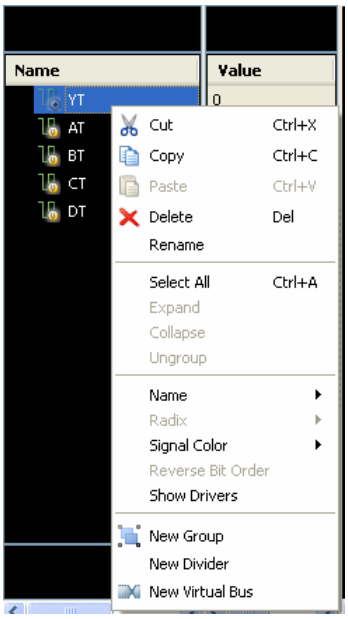
This displays the useful part of the simulation. Use the magnifying glass with the plus sign to zoom in further, as follows:



On the left side of the simulation panel there are columns labeled Name and Value:



For a given item on these columns, you can right-click and choose options to delete, rename, or change the color of the signal color.



You may also use the scroll bars to see the simulation at different times as well as observe more signals if you have a larger design.

The simulation control option on the top right side of the ISim toolbar contains the following features:

1. Restart simulation by stopping it and setting time back to 0.
2. Run simulation until all events are executed.
3. Run simulation for a specified time indicated by the Value box.
4. Amount of time and unit simulation is to run for.
5. Run simulation for one executable HDL instruction at a time.
6. Pause simulation.
7. Stop simulation.

Changing Stimulus

If you have different cases of stimulus that you wish to try out in the simulator, simply close ISim, edit the Verilog test fixture in ISE's text editor, and rerun the Simulate Behavioral Model process to open ISim again.